REMARKS

File History

In the latest substantive Office action of 04/06/2005, the following allowances, rejections, objections and other actions appear to have been made:

> Claims 11 and 46-52 were allowed.

> Claims 43-44, 56-58 were objected to, but indicated to contain allowable subject matter.

> Claims 1-10, 12-16, 19-20, 23-25, 28-30, 33-36, 39-41, 45, 53-55 were rejected under 35 USC §102(e) as each being fully **anticipated** by newly-cited Vassiliev et al (US 6,583,069 based on an application filed 12/13/1999);

> Claims 6-7, 17-18, 21-22, 26-27, 31-32, 37-38, 42 were rejected under 35 USC §103(a) as each being **obvious** over newly-cited Vassiliev et al and in further view of PTO provided comments;

> The application Status sheet (page 1) of the Office action (OA) was marked as constituting a "final" action even though no reasons were given for finality and no indication was made elsewhere that the Examiner was making this action final. It should be noted that previous grounds of rejection have been withdrawn by the PTO and that Vassiliev '069 is a newly cited reference which Applicant is responding to for the first time. Thus no issues have been clearly created between Applicant and the PTO with regard to newly-cited Vassiliev or its applicability to each of the claims.

Summary of Current Response

Claims 1, 12, 40, 43 and 56 are amended.

Claims 2 and 13 are cancelled.

Arguments are presented concerning the applied art and its proposed combination.

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Given that no reason is given for finality, final status is inappropriate and Applicant takes it that the Status sheet marking was an inadvertent error. See MPEP §706.07 ("Before final rejection is in order a clear issue should be developed between the examiner and applicant. .... The final rejection letter should conclude with Form Paragraph 7.39."); and MPEP §706.07(a) ("Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement").

Applicants' Reading of Newly-Cited Vassiliev '069 and Overview of Outstanding Office Action

Applicant agrees that Vassiliev Fig. 1 (labeled Prior Art) schematically illustrates openings of different widths and heights.

However these openings are formed in **silicon oxide film 103**, and only as that oxide is being sputter deposited on top of itself and on top of underlying "steps 102" of equal height where the latter "steps" are formed on an apparently planar, semiconductor substrate 101. (Vassiliev col. 1, line 44).

Vassiliev does not teach or suggest making trenches of different depths or widths in a semiconductor substrate. Quite the opposite, Vassiliev shows the semiconductor substrate 101 of Figs. 1 and 7 to be planar with equal height "steps" of unknown but different composition formed on top of this planar semiconductor substrate 101 and then oxide deposited between the "steps". During the sputtering process, the partially-completed sputtering itself defines the varying contours of the being-deposited, oxide 103, 104, 107.

Most of the outstanding grounds of rejection are based on the erroneous assumption that Vassiliev discloses trenches of different aspect ratios defined in a semiconductor substrate (OA page 2, first sentence after the 102(e) rejection). Nothing in Vassiliev's disclosure validates a finding that trenches of different aspect ratios are defined in Vassiliev's semiconductor substrate.

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Vassiliev states at col. 1, line 17:

> For the purpose of this disclosure, the substrate includes a bulk material such as semiconductor, e.g., silicon, body, and if present, various regions of materials such as dielectric materials, conducting materials, metallic materials, and/or semiconductor materials. One of the material regions utilized in this fabrication procedure includes a silicon oxide, i.e., a material represented by the formula SiO_n, where n=~ 2, or doped silicon oxide films, containing an additional doping element such as boron, phosphorus, fluorine, carbon, and their mixtures with total dopant content depending on the purpose of film application in the device. Below, the common term "silicon oxide film" is used to characterize both silicon dioxide films and silicon oxide based glass films. Silicon oxide regions are utilized as insulating/passivating layers; as an electrical insulation **between** conducting **layers**, e.g., polysilicon or metal layers. Films of undoped silicon oxide are used also as a liner or as a cap layer either under or on the doped silicon oxide layers, respectively, to limit unacceptable dopant migration during subsequent processing.
>
> [emphasis added]

It is clear from the above that Vassiliev's teachings are limited to silicon oxide that is used as an inter-layer insulator.

It is even clearer that Vassiliev is a prophetic filing in which the inventors "propose" (col. 8, lines 58 and 66) to include certain "**additives**" into any standard HDP-CVD reactor (see col. 7, lines 22-29) so as to alter the intermediate chain reaction byproducts (IMPs' of col. 8, line 10). They make "estimates" of ranges to be used. The etch-to-deposition ratio is not controlled according to Vassiliev, but rather it is the inclusion of the proposed additives that is believed to produce voidless deposition over the possible operating range of any of the stated standard HDP-CVD reactors (see again col. 7, lines 22-29).

Thus, Vassiliev is not teaching to "control" the etch-to-deposition ratio as the PTO alleges. Vassiliev is merely listing the etch-to-deposition ratio range of the standard reactors. It is impermissible to make an obvious-to-try rejection. Just because a reactor is capable of certain values with a range, that alone does not make it obvious to practice every possible value within the available range.

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More importantly, Vassiliev teaches "To improve undesirable bread-loaf shape 301 in FIG. 6A, an increase of etch to deposition ratio is normally used." (col. 8, line 38). Thus, Vassiliev is teaching away from going to the lowest etch-to-deposition ratio available from commercial reactors.

In view of the above, it is respectfully submitted that a prima facie case of unpatentability has not been made out.

The Current PTO position

Looking closer at the details, the outstanding Office action appears to assert that each and every limitation of Claims 1-10, 12-16, 19-20, 23-25, 28-30, 33-36, 39-41, 45, 53-55 is clearly present in Vassiliev '069.

However, as pointed out above, the foundational assumption about Vassiliev having trenches defined in a semiconductor substrate is clearly eeroneous.

With respect to **Claim 1** (as amended above), Vassiliev does not disclose "(c) controlling the etch and the deposition ... such that a nonzero etch to deposition ratio of 0.025 or less is established". The "Estimated" range in Vassiliev Table 1 (cols. 3-4) is merely a prophetically "proposed" broad range without any indication that it should be controlled to establish a value below a specified magnitude.

With respect to **Claim 3**, the allegation of there being an oxygen to silane ratio recited in the Abstract is unfounded. Vassiliev is talking about his special **"additives"** and those are specified at cols. 11-12 (Table-4 continued). Oxygen is not recited as one of the "additives".

With respect to **Claim 10**, it has not been shown without speculation that the "steps" of Vassiliev metal. Moreover, once again, Vassiliev does have trenches in a semiconductor substrate.

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With respect to **Claim 14**, see comment re Claim 3.

With respect to **Claim 19**, see comment re Claim 3 and note additionally that no finding of fact has been made regarding the recited step "(b) controlling a bias signal ...". In order to make a valid anticipation rejection, it must be shown that each and every limitation is present.

With respect to **Claim 24**, there has been no showing that one of Vassiliev's trenches is twice as wide as another. It is well known that patent drawings are not to scale unless specifically so stated. Moreover with regard to Claim 24, there has been no showing of a ratio of oxygen inflow rate to silane inflow rate of 1.7 or less combination with the total flow rate of the silane, oxygen, and inert gasses being 500 standard cubic centimeters per minute or more. Vassiliev's Tables do not establish specific combinations. They merely "propose" ranges over which the hypothesized additives might work. Moreover with regard to Claim 24, there has been no showing of a step of "(b) controlling a bias signal". The outstanding grounds of rejection are completely silent re the last item. Thus a prima facie case of unpatentability is not present and finality is clearly premature.

With respect to **Claim 29**, there has been no showing of any one or more of: "trenches defined in a semiconductor substrate"; "a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less"; and "controlling a bias signal".

With respect to **Claim 35**, there has been no showing of any one or more of: "a first trench is at least twice as wide"; "(a) using silane ... and a helium gas" (note: although Table 1 of Vassiliev lists He as a possible carrier gas, it is part of a long list with no specific combination called out); and "(b) controlling a bias signal which affects a sputter etch action of the helium gas ...".

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With respect to **Claim 39**, there has been no showing that Vassiliev restricts the total flow including that of the carrier gas, Vassiliev Table 1 allows for 400 sccm of carrier gas. This combined with the 400sccm of oxygen exceeds 625. Even the "most preferred" combination of Vassiliev Table 1 allows for more than 625sccm (200+350+100=650). An anticipation rejection requires absolute certainty, not speculation.

With respect to **Claim 53**, there has been no showing of "thereby provid[ing] a substantially planar set oxide-filled trenches upon which other layers of material are founded" [bracketed text inserted for readability]. All of Vassiliev's diagrams show that non-planar upper surfaces are formed.

With respect to **Claim 55**, there has been no showing of "within about 600Å ".

Comments re Obviousness Rejections

With respect to the summary dismissal of remaining claims as being obvious over Vassiliev on the unsupported speculation that the isolation of improvements or optimal results requires "only routine skill in the art" (citing In re Aller), Applicant respectfully disagrees.

Under this logic, all "discovery" type inventions would be unpatentable. However, 35 USC §100 clearly states that "(a) The term ``invention" means invention or discovery." [underlining added]. 35 USC §101 clearly states that "Whoever invents or discovers any ... or any new and useful improvement thereof, may obtain a patent therefore" [underlining added]. There are no per se rules regarding what is obvious or not with respect to all inventions. Instead the PTO must necessarily make specific findings of fact supported by evidence of record. See In re Sang-Su Lee 61 USPQ2d 1430 (Fed. Cir. 2002). There is no evidence of record in the present case, just unsupported, raw conclusions of obviousness.

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Moreover, Vassiliev teaches to use "additives" as the primary means for avoiding void formation. Vassiliev does not teach how to control the etch-to-deposition ratio. It is not

understood how the PTO can summarily decide that all discoveries are a matter of routine experimentation.

CONCLUSION

In light of the foregoing, Applicant respectfully requests that the rejections be withdrawn. Should any other action be contemplated by the Examiner, it is respectfully requested that he contacts the undersigned at (408) 392-9250 to discuss the application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 1, 2005.

[signature] 7-1-2005

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Respectfully submitted,

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